Optimization of Analog Fault Coverage by Exploiting Defect-Specific Masking

Anthony Coyette†, Ronny Vanhooren‡, Wim Dobbelaere‡ and Georges Gielen†

†Department of Electrical Engineering, KULeuven, Belgium
‡ON Semiconductor Belgium
{anthony.coyette, georges.gielen}@esat.kuleuven.be
{ronny.vanhooren, wim.dobbelaere}@onsemi.com

***Abstract*—A new method is presented to detect catastrophic defects from the signal analysis of dynamic current consumption waveforms of analog circuits. While other techniques use the whole information in a Root-Mean-Square computation or in black-box techniques such as a neural network, the central point of this work resides in the selection of waveform samples to create a signature able to discriminate a defective circuit from a fault-free circuit. The selection of samples is implemented by the introduction of binary vectors to partially mask the data. Confronted with process variations, this technique offers the advantage of being straightforward and simple to implement in Automated Test Equipments. The generation of the masks is optimized to improve the defect coverage by means of a genetic algorithm maximizing the distance between the signature of the fault-free circuit and a faulty circuit. Results from simulations on industrial circuits show that the number of detected defects can be nearly doubled for specific stimuli.**

Index terms – Structural testing, power supply current monitoring, dynamic current monitoring.

I. Introduction

The large increase of the number of silicon chips inside modern applications such as automotive has created an increasing interest to avoid electronic malfunctions in the field [1]. The current state of the art for complex mixed-signal ASICs is of the order of 1 PPM test escapes. Although the number of transistors in the digital core usually outnumbers the number of analog transistors by an order of magnitude, the observed digital test escapes are typically below 100 ppb. The dominant remaining portion of customer returns in industry can be traced back to silicon defects in the analog circuitry that are not caught by the test program. Although the digital core is a dense part of the device under test, a very good quality can be achieved because of the use of a structured test approach with scan insertion and a combination of stuck-at, bridging, Iddq and transitional ATPG patterns [2]. For the analog blocks, on the other hand, there are no automated structured approaches existing today and the industry standard is to rely on functional 100% specification testing of analog blocks to meet the quality requirements.

This superiority in the defect coverage in the digital domain has led to the transposition of digital test techniques to the analog field. First, by the use of a fault model, Milor reduced the size of test sets in [3]. In the family of structural test techniques the power supply current has been used for a long time to detect defects in digital circuits [4]. Then in [5], Camplin and al. used the Iddq technique to unify the testing of analog and mixed-signal circuits. The analysis of the supply has been studied for dynamic consumption by [6] in the time and frequency domains. [7] proposed the same analysis for different power supply signals and [8] an optimization on the power supply. Lately, new tools coming from mathematics have been applied to the field. Studies like [9] [10] make use of the wavelet decomposition analysis and [11] [12] propose detection methods based on neural networks.

The present paper is proposing a structured method to improve the analog fault coverage by simulating each potential defect and creating defect-specific test masks that allow to improve the observability of potential defects. The advantage of this method is threefold. First, in comparison to other methods, the detection does not work on a single threshold but relies on the information generated for each defect specifically. Secondly, the problem is formulated in a white-box approach with a clear optimization criterion, and avoids the use of black-box approaches such as neural networks. Finally, the proposed approach generates a binary vector that is easy to implement on any ATE and makes it a straightforward method to increase the analog fault coverage in practice.

The remainder of the paper is structured as follows. Section II reviews the concept of defect-oriented current monitoring while Section III presents the developed testing method as an improvement to the state-of-the-art in analog fault coverage. Section IV presents the results of the method simulated for an example circuitry. Section V concludes.

II. Defect-Oriented Analog Testing

The adopted approach in testing follows the tracks of other works applying the Simulate-Before-Test methodology (SBT) like in [13]. On the basis of fault models representing the physical defects and the simulation of their impact on the circuit, useful information is extracted aiming the test of chips after fabrication.

The implemented software framework, illustrated in Figure 1, injects one by one the faults into the circuit netlist and simulates the behavior of the resulting circuit responding to pre-defined stimuli. The information used from those computations is the power supply current consumption waveform of the circuit. The central idea of this paper being a general

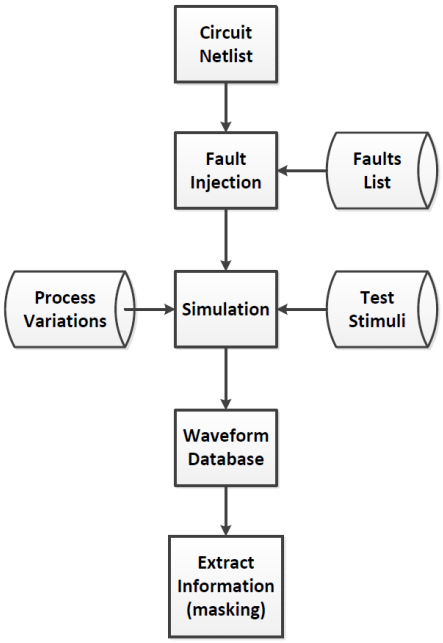

Fig. 1. Flow of analog test methodology using defect-specific masking

methodology, this framework can be extended to the extraction of other waveforms such as the node voltages. If these nodes are input or output of the circuit, their observability poses no problem contrary to internal nodes. The case of internal nodes requires generally the use of Design-for-Testability.

The used faults database is built from the schematic of the targeted circuit, but could be extended to methods using the Inductive Fault Analysis (IFA) [14] taking advantage of the information offered by the layout showing the spatial structure of the circuit. In the scope of this work, the focus is put on defects occurring in the transistors themselves and the 6-faults model of Figure 2 is applied to every transistor appearing in the schematic. This model is a classic 5-faults model as in [15], to which the open-gate (base) fault is added, resulting in the set of 6 possible faults : open gate (base), open drain (collector), open source (emitter) and source-drain (emitter-collector), drain-gate (collector-base), source-gate (emitter-base) shorts. The result of this fault generation is stored in a database of defective circuits $FL = \{F_1, F_2, ..., F_K\}$ where K is the total number of possible defects.

After simulation taking into account process variations, the waveforms are stored as vectors of samples. The method proposed in the next section relies on the data stored in that database. Note that although the power supply current is used as stored waveform in this paper, the methodology presented of course also applies to other waveforms.

III. Defect-Specific Masked-RMS Monitoring

In case the process variations would be neglected, let us define the fault-free circuit G to which the continuous power input signal S(t) is applied, resulting in the continuous supply current consumption X(t). Now, as the effect of the process variations is taken into account, a family of N circuits is considered instead of one circuit. Let us define G_i as the i^{th} variation of G under process variations and $X_i(t)$ its corresponding supply current consumption with i=1,...,N. Similarly, $F_{i,j}$ indicates the i^{th} variation of the j^{th} faulty circuit from the list FL. The same input applied to $F_{i,j}$ gives the supply current waveform $Y_{i,j}(t)$. In the following, the terminology $X_i[z]$ is used to refer to the vectors of samples resulting from the measurement of the corresponding waveforms, which are the data used during the computations, and where z=1,...,Z with Z the number of samples.

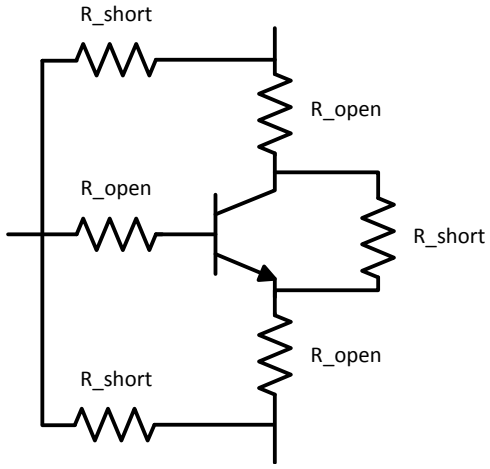

Fig. 2. 6-fault model of a transistor.

Following the existing dictionary-based methods [13], this methodology proposes the construction of a defect-detection scheme built on the simulation of all possible defects and the recording of specific signatures provoked by the applied inputs. Standard analysis techniques typically opt for the Root-Mean-Square (RMS) value of transient signals like the output voltage or the current supply to discriminate between fault-free and faulty circuits. The Root-Mean-Square (RMS) value of a waveform X[z] is calculated according to [16] as :

$$RMS(X) = \sqrt{\frac{1}{Z}\sum_{j=1}^{Z} X[j]^2}. \quad (1)$$

Calculating the RMS value for every X_i gives a distribution $pdf_{RMS(X)}$. The distributions obtained from the family of fault-free circuits and from the families of defective cases can lead to a decision threshold as in [6]. In the current paper, a defect-specific signature computation is introduced. The central idea of this method is to use the knowledge of where defects can physically occur and express themselves, to focus the data collection on specific information in order to maximize the fault discrimination. This focus is obtained by introducing a mask which selects information that according to the design simulations are not influenced by a defect and it draws attention to the data points that can be influenced by a defect. The RMS formula is re-used while the masking m_j is introduced to give :

$$RMS_{masked}(X, M) = \sqrt{\frac{\sum_{j=1}^{Z} m_j X[j]^2}{\sum_{j=1}^{Z} m_j}}. \quad (2)$$

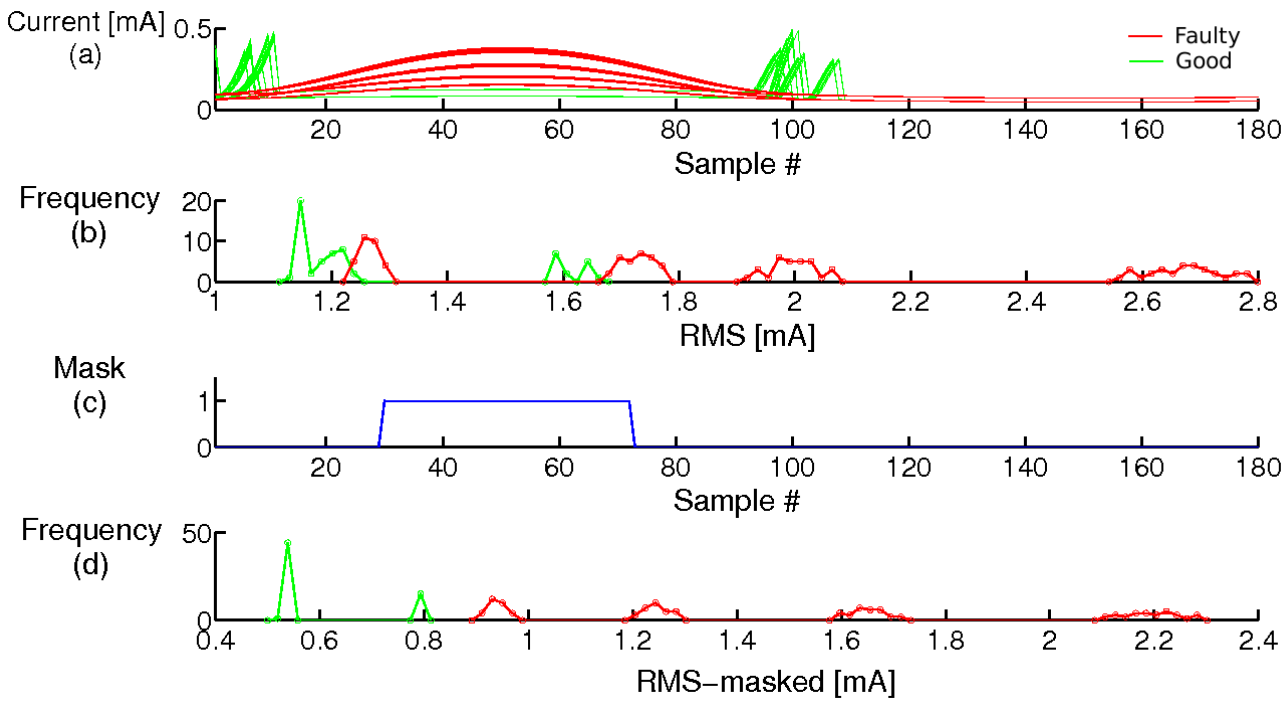

Fig. 3. Separation by the no-overlap criterion :
(a) family of waveforms for the fault-free circuit and for a defective one.
(b) histograms of the RMS values of the waveforms.
(c) mask generated by the no-overlap criterion.
(d) masked RMS values showing that the distributions are separated.

where $m_i \in \{0,1\}$ for i=1,...,Z are the values of the mask $M = (m_1, ..., m_Z)$.

The general algorithm proceeds in two phases : a training phase and a test phase. The former makes use of the waveforms generated a priori by the simulations to define the K masks M_k and the K thresholds Th_k to apply. The latter applies applies the masks M_k to the ATE waveforms measured from the manufactured chips and tests the values against the corresponding threshold Th_k.

Algorithm 1 Training Phase

A. Compute the $pdf_{X[z]}$ distributions of N fault-free circuits
for each defective circuit k=1,...,K **do**
B. Compute the $pdf_{Y_k[z]}$ distributions of N defective circuits
C. Compute the Z values m_k of the mask M_k
D. Compute the decision threshold Th_k
end for

Algorithm 2 Testing Phase

for each mask k=1,...,K **do**
A. Compute RMS_{masked}
B. Test RMS_{masked} against Th_k
if Test positive **then**
C. Sort CUT C as defective
D. Stop
end if
end for

The manner to compute the masks is explained in the next section. For the thresholds computation, an overlap of the two distributions does not allow to decide with certainty if the circuit has a defect or not. According to the Bayesian theory of detection, a minimization of the risk of misclassification leads to an optimal threshold [17]. But in the scope of this work, a simpler and more pessimistic criterion is applied. If the two distributions overlap, the defect is classified as undetected. If the two distributions do not overlap, the defect j can be detected and the decision threshold Th_j is chosen as the center of the space separating the two distributions :

$$Th_j = \frac{1}{2}\Big(\min_{i\in\{1,...,N\}} RMS_{masked}(X_i, M) + \max_{i\in\{1,...,N\}} RMS_{masked}(F_{i,j}, M)\Big) \quad (3)$$

In the following algorithms, empirical probability density functions are used. These are computed from the simulation results in order to avoid any hypothesis on the Gaussian nature of the considered distributions. It is also noteworthy that while the next section is explained in the time domain, the same flow can be applied to the frequency domain or any time-frequency representation such as the Wavelet Analysis, or the Walsh-Hadamard transform.

A. Mask defined by non-overlapping distributions

In a first version, the construction of the masks is based on a direct analysis of the problem. For every time step z_l, the N

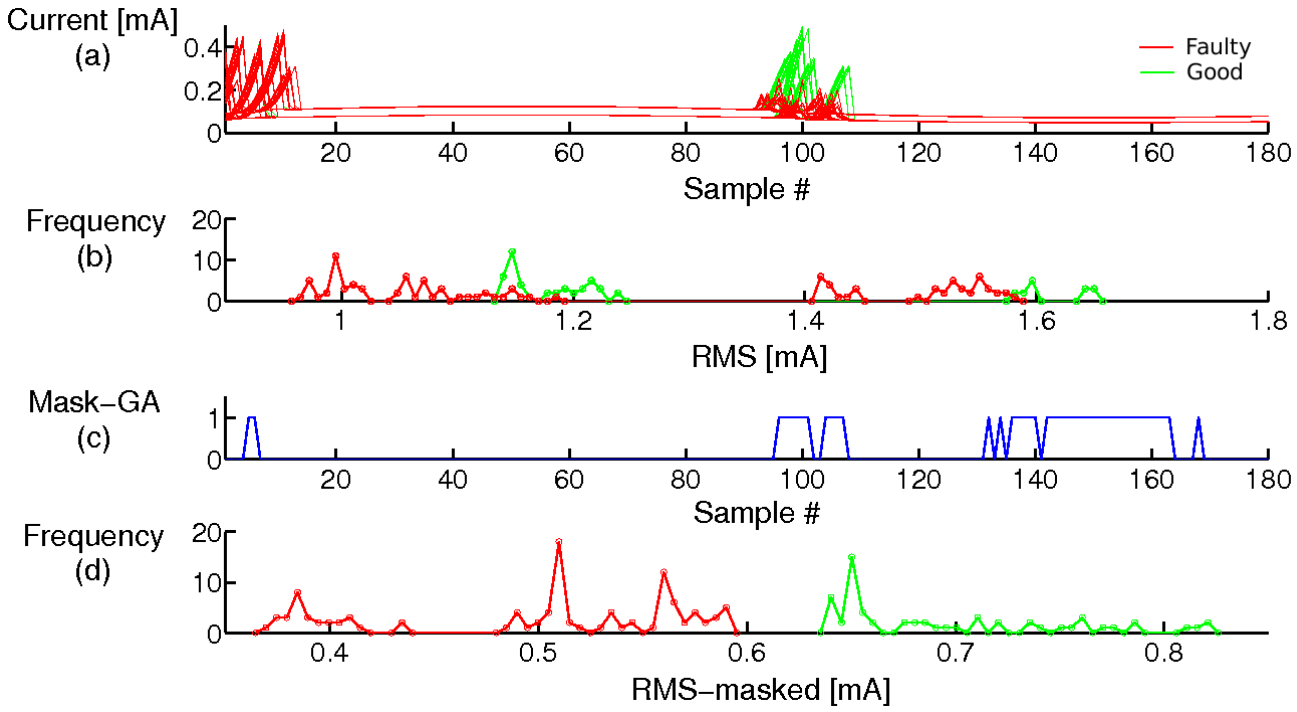

Fig. 4. Separation by genetic algorithm :
(a) family of waveforms for the fault-free circuit and for a defective one.
(b) histogram of the RMS values of the waveforms.
(c) mask generated by the genetic algorithm.
(d) masked RMS values showing that the distributions are separated.

values $X_i[z_l]$, which are the $z_l{}^{th}$ samples of the N fault-free circuits G_i, are considered to form the distribution $pdf_{X[z_l]}$, where $z_l = 1, ..., Z$. Then, for every defective circuit F_j of the list FL, and for every time step z_l, the N values $Y_{i,j}[z_l]$ are considered to form the distribution $pdf_{F_j[z_l]}$. In total, Z and Z×N distributions are considered respectively for the fault-free case and the faulty cases. The Z values of the mask for the defective circuit F_j, $M_j = (m_1, ..., m_Z)$ are defined as :

$$m_{z_l} = \begin{cases} 1 & \text{if } pdf_{Y_j[z_l]} \cap pdf_{X[z_l]} = \emptyset \\ 0 & \text{otherwise} \end{cases} \quad (4)$$

The direct use of masks as defined here allows to separate in some cases the distributions for the faulty and fault-free cases. Figure 3 illustrates this by showing two families of waveforms : the waveforms resulting from the fault-free circuit and those from a defective circuit; both produce a family of waveforms because of the process variations. The second graph shows the two histograms formed by the RMS values of every waveform. Because of the process variations, the computation of the RMS value of a waveform leads sometimes to the impossibility to decide whether the circuit is faulty or not. But by the introduction of the a mask proposed in the third graph to hide some samples, one can see that the results in the separation of the two masked RMS distributions in the final graph.

B. Mask optimization by Genetic Algorithm

In order to further improve the coverage, the mask selection is now formulated as an optimization problem as follows. On the basis of the simulated waveforms, the best mask is the one which allows the best separation of the two RMS-masked distributions :

$$M = \max_{m \in \{0,1\}^Z} \Delta(F_j, G, m). \quad (5)$$

where Δ is a function expressing the distance between the two distributions obtained by the RMS-masked values of the N waveforms from G_i and F_j using the mask m :

$$\Delta(F_j, G, m) = \min_{i \in \{1,...,N\}} RMS_{masked}(G_i, m) - \max_{i \in \{1,...,N\}} RMS_{masked}(F_{i,j}, m). \quad (6)$$

This definition of distance between the two distributions is a computationally efficient simplification of the problem in the case of using the no-overlap detection criterion introduced in Section III. The detection of a defect in the case of overlapping distributions with a Bayesian decision threshold would require a finer computation of the distance between the two distributions, as for example the Bhattacharyya distance [18].

The optimization problem stated here has been solved by a genetic algorithm. Such an algorithm has already been used in the past for the test of analog circuits and is described in works like [19] [20]. The choice of using a genetic algorithm is motivated by the size of the solution space and the non-linearity present in the definition of the distance between two distributions subject to masking.

As a result, Figure 4 illustrates a case where the RMS value cannot discriminate the faulty from the good case and the mask generated by the no-overlap criterion is not able to separate the two distributions. But the optimized mask found by the genetic algorithm manages to select a subset of samples allowing to discriminate the faulty case.

IV. Experimental Results

The proposed approach has been applied to an industrial Power-On-Reset (POR) circuit (Figure 5) designed in the 0.35 μm BCD technology I3T50 [21]. As shown in Figure 2, the defect-oriented test is applied by using a resistor-based fault model. A value of 100 Ω was chosen for the resistors modeling the shorts and 100 MΩ for the resistors modeling the opens.

In order to take the inter-die and intra-die process variations into account, a Monte-Carlo simulation of 15 samples is carried out for the 8 different corners. These 8 corners result from the different combinations of the extreme values indicated by the technology files for the resistors, MOS and bipolar transistors. Therefore, the final database consists of a total population of 120 waveforms for the fault-free circuit and for every possible defective case. All these waveforms are recorded as vectors of values resulting from a sampling at 200 kS/s applied to the simulated transient waveforms (power supply current in this paper). This sampling frequency is in line with the capabilities of a state-of-the-art industrial ATE. The amplitude quantization losses are not taken into account for this work.

Example : Power-On-Reset Circuit

The Power-On-Reset circuit, shown in Figure 5, is a basic element appearing in many integrated circuits, allowing the reset of the registers and enabling startup in a predefined configuration. This circuit does not stand as a generally used benchmark but constitutes an important block that should be fully covered because of its critical utility in mixed-signal chips. To demonstrate the added value of the presented method, the results are compared for three cases and three different signals. The three cases are the simple RMS value and the two masked-RMS values with the mask generated by the two different methods discussed. The waveform measured is the power supply current. The signals applied to Vdd are sinewaves of the form :

$$S_i(t) = V_i + A_i sin(2\pi f_i t)$$

where i $\in \{1,2,3\}$, V_i is the offset voltage, A_i the amplitude, f_i the frequency and t the time. The 3 sets of values used are :

$$\begin{array}{lll} V_1 = 2.8\text{V}, & A_1 = 0.5\text{V}, & f_1 = 5\text{kHz} \\ V_2 = 1\text{V}, & A_2 = 0.5\text{V}, & f_2 = 1\text{kHz} \\ V_3 = 2\text{V}, & A_3 = 2\text{V}, & f_3 = 500\text{Hz} \end{array}$$

The first and third signals applied on the power supply make the Schmitt Trigger pass from one state to another in both ways : High to Low and Low to High. The second signal does not cause such a property and is shown here to prove the concept in a general case. The goal here was not to provide an optimization on the stimuli itself like in [8], but an improvement on the measured waveform processing leading to a better coverage for given stimuli.

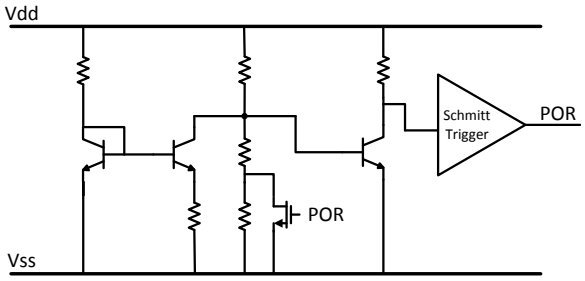

Fig. 5. Schematic of the Power-On-Reset circuit.

According to the 6-fault model introduced in Figure 2 and the schematic given in Figure 5, 94 possible defects are considered.

The results shown in Figure 6 show how many defects are detected by the different methods for each of the stimuli. The first method is a simple computation of the RMS value from a waveform; the second relies on the RMS-masked value demonstrating that the masking of specific samples from the waveform allows the detection of defects that are not caught by using a simple RMS signature. The gain obtained by the introduction of a mask is noticeable for the three cases.

While the direct method improves the coverage and states clearly where the useful information resides in the waveforms, the genetic algorithm optimization achieves a much better coverage but loses some insight in the precise location of the information. In both cases, the implementation on ATEs remains straightforward and catches 67 defects when the results of the three signals are combined. In particular, Figure 6 shows that the fault coverage is increased from less than 30 faults with the no-mask method up to about 60 detected faults when using masking, i.e. a doubling of the fault coverage. Further increase of the fault coverage requires more input stimuli and/or output waveforms to be considered.

Finally, to support the scalability of this method, the concept must be combined with Design for Testability techniques. The present example contains 15 transistors and the simulation time is not a problem. However this can not be directly applied to large circuits due to the intractability of the simulations. The usage of the intrinsic hierarchy in complex integrated circuits containing more transistors can be used for a partitioning approach as proposed in [22]. When considering a whole system with many sub-circuits, the different blocks can be made independent from each other by controlling their inputs with pass-gates. This non-dependency allows to only simulate the isolated parts and keeps the simulations tractable.

V. Conclusion

A new method has been proposed to improve the analog fault coverage of mixed-signal integrated circuits. By using defect-specific masks it is possible to detect catastrophic defects that cannot be observed using a standard computation of the RMS value of the measured waveforms.

The technique is based on simulating each potential defect and creating a defect-specific test mask. These binary masks

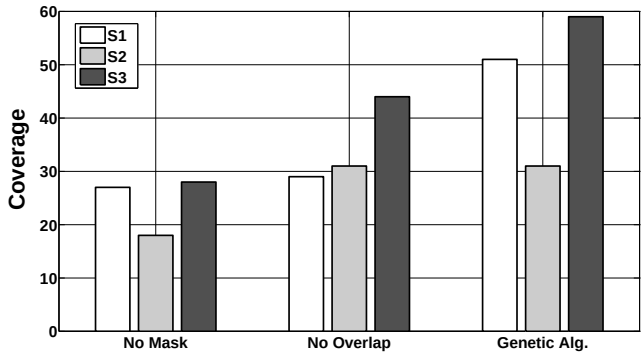

Fig. 6. Comparison of the fault coverage of the 3 methods for the 3 test stimuli S_1, S_2, S_3.

are multiplied with the measured test data in order to increase the distance between the RMS distributions of good and bad circuits and hence to achieve an improved defect observability. The defect-specific masking technique has been applied to an industrial Power-On-Reset circuit and it was demonstrated that the number of detected defects for a given test stimuli can nearly be doubled compared to the traditional RMS computation.

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